JC02 Rec'd PCT/PTO 22 DEC 2000

FORM PTO-1390
(REV. 1-98)

U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
3672-0110P

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
09/720329 NEW

INTERNATIONAL APPLICATION NO.	**INTERNATIONAL FILING DATE**	**PRIORITY DATE CLAIMED**
PCT/NO00/00127	April 14, 2000	April 22, 1999

TITLE OF INVENTION
A METHOD IN THE FABRICATION OF ORGANIC THIN-FILM SEMICONDUCTING DEVICES

APPLICANT(S) FOR DO/EO/US
ROMAN, Lucimara Stolz; INGANAS, Olle; HAGEL, Olle; BERGGREN, Magnus; GUSTAFSSON, Goran;*

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau). WO 00/65653
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(3)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98./International Search Report with cited references
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    Request (PCT/RO/101)
    Eight (8) sheets of formal drawings

*CARLSSON, Johan

528 Rec'd PCT/PTO 22 DEC 2000

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/720329	PCT/NO00/00127	3672-0110P

17. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO............ **$1,000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO........ **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO............ **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)............ **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)................ **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 1,000.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☒ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	17 - 20 =	0	X $18.00	$ 0.00	
Independent Claims	1 - 3 =	0	X $80.00	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		No	+ $270.00	$ 0.00	

TOTAL OF ABOVE CALCULATIONS =	$ 1,130.00		
Reduction of ½ for filing by small entity, if applicable. Applicant claims Small Entity Status in accordance with 37 CFR 1.27.	$		
SUBTOTAL =	$ 1,130.00		
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$		
TOTAL NATIONAL FEE =	$ 1,130.00		
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$		
TOTAL FEES ENCLOSED =	$ 1,130.00		
	Amount to be: refunded	$	
	charged	$	

a. ☒ A check in the amount of $ 1,130.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account. No. __________ in the amount of $______ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2448.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:

Birch, Stewart, Kolasch & Birch, LLP or Customer No. 2292
P.O. Box 747
Falls Church, VA 22040-0747
(703)205-8000

SIGNATURE

MUTTER, MICHAEL K.
NAME

#29,680 (MKM)
REGISTRATION NO.

/djm 12/22/00

(REV. 12/11/2000)

PATENT
3672-0110P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:	ROMAN et al.		
Int'l. Appl. No.:	PCT/NO00/00127		
Appl. No.:	NEW	Group:	
Filed:	December 22, 2000	Examiner:	
For:	A METHOD IN THE FABRICATION OF ORGANIC THIN-FILM SEMICONDUCTING DEVICES		

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

December 22, 2000

Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in connection with the above-identified application.

AMENDMENTS

IN THE SPECIFICATION:

Please amend the specification as follows:

Before line 1, insert --This application is the national phase under 35 U.S.C. § 371 of PCT International Application No. PCT/NO00/00127 which has an International filing date of April 14, 2000, which designated the United States of America.--

IN THE CLAIMS:

Claim 10, line 1, change "claims 7 and 8" to --claim 7--

Claim 16, line 1, change "any of the claims 1-15" to --claim 1--

Claim 17, line 1, change "any of the claims 1-15" to --claim 1--

REMARKS

The specification has been amended to provide a cross-reference to the previously filed International Application.

The claims has been amended merely to remove the multiple dependencies and to place the application into better form prior to examination.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By ______________________________
Michael K. Mutter, #29,680

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

MKM/djm
3672-0110P

PATENT
3672-0110P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: ROMAN et al.

Appl. No.: New Group:

Filed: December 22, 2000 Examiner:

For: A METHOD IN THE FABRICATION OF ORGANIC THIN-FILM SEMICONDUCTING DEVICES

INFORMATION DISCLOSURE STATEMENT (SUBMISSION CONCURRENT WITH THE FILING OF A NEW PATENT APPLICATION)

Assistant Commissioner for Patents
Washington, DC 20231

December 22, 2000

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

II. COPIES

☒ Submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

☐ This application is a National Phase of a PCT application. Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should be forwarded from the International Search Authority. If copies are needed, please contact the undersigned.

III. <u>CONCISE EXPLANATION OF THE RELEVANCE</u>
(check at least one box)

a. ☒ **DOCUMENTS IN THE ENGLISH LANGUAGE**

The attached patents, publications, or other information in the English language do not require a statement of relevancy.

b. ☐ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

c. ☐ **ENGLISH LANGUAGE SEARCH REPORT**

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(A)(3).

d. ☐ **OTHER**

The following additional information is provided for the Examiner's consideration.

Docket No. 3672-0110P

FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If The Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule (with a petition if necessary) and charge the appropriate fee to Deposit Account No. 02-2448.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By ______________________
Michael K. Mutter, #29,680

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

MKM/djm
3672-0110P

Enclosures:

- ☒ Form PTO-1449(s)
- ☒ Documents
- ☐ Foreign Search Report
- ☐ Fee
- ☒ Other: International Search Report

(Rev. 04/19/2000)

A method in the fabrication of organic thin-film semiconducting devices

The present invention concerns a method in the fabrication of an organic thin-film semiconducting device, wherein the semiconducting device comprises an electrode arrangement with electrodes contacting the semiconducting organic material.

The invention also concerns applications of the method according to the invention.

Particularly the invention concerns the modification of the injection properties of electrodes in an electrode arrangement for a semiconductor component manufactured with organic semiconducting material.

A paper by M. Granström & al.. "Laminated fabrication of polymeric photovoltaic diodes", Nature, Vol. 395, pp. 257-260, discloses a photovoltaic diode with a double layer of semiconducting polymers. Photoexcited electron transfer between donor and acceptor molecular semiconductors provides a method of efficient charge generation after photoabsorption and can be exploited in photovoltaic diodes. But efficient charge separation and transport to the collector electrodes are problematic, because the absorbed photons must be close to the donor-acceptor heterojunction, while at the same time good connectivity of the donor and acceptor materials in the respective electrodes is required. Mixtures of acceptor and donor semiconducting polymers can provide phase-separated structures which to some extent meet this requirement, providing high photoconductive efficiencies. To this end Granström & al. disclose two-layer polymer diodes where the acceptor material is a fluorescent cyano derivative of poly(*p*-phenylene vinylene) (MEH-CN-PPV) doped with a small amount of a derivative of polythiophene (POPT). The acceptor layer is contacted by an electrode and covered by a glass substrate. The acceptor layer is laminated together with a donor layer of POPT doped with a small amount of MEH-CN-PPV which is spin-coated on either indium tin oxide (ITO) substrates or glass coated with polyethylene dioxide thiophene (doped with polystyrene sulphonic acid) (PEDOT-PSS). To ensure a low contact resistance a thin layer of gold was thermally evaporated on the glass substrate before the PEDOT material was spin-coated thereon. Since Granström & al. describe a photovoltaic diode, it is evident that they are not concerned with obtaining a high rectification ratio such as will be desirable in switching

diodes, nor is a difference in the work function values of the cathode and the anode an issue, although the materials envisaged for the anode, ITO, PEDOT and gold all have a high work function value, ranging from 4,8 for ITO to well above 5 eV for PEDOT and gold, the work function values of the latter two being almost similar.

However, it has been found that particularly noble metals such as gold and platinum cause in a poor quality of a conducting polymer thin film deposited thereupon and very often the polymer film presents pin holes which are not acceptable when the films are arranged in a sandwiched geometry. Moreover gold is a costly material, but apparently Granström & al. have selected gold because of its high work function value matching that of PEDOT-PSS.

In switching semiconductor devices with diode structures a high rectification ratio at of the latter will be desirable and it is also desired that the contact surface between an electrode and a semiconducting polymer should provide efficient charge injection, but this latter feature is not of concern for collector electrodes, that are the anodes, in a photovoltaic device based on organic semiconducting materials.

It is known that the contact surface between a conducting and a semiconducting polymer has superior properties with respect to injection of charge. For example a conducting polymer based on poly(3,4-ethylenedioxythiophene) (PEDOT) possesses a very high work function which makes it suitable as anode in semiconductor components based on organic semiconductors, but the high resistivity of PEDOT limits the performance of components because of a very high series resistance. This is particularly unfortunate when the electrodes are patterned with line widths of the order of 1μm. However, it is believed that such components shall be crucial to realizing high density memory cells for use in memory modules based on polymer as the memory material, provided that it will be possible to achieve the desired high data read-out speed. This shall, however depende on the possibility of highly conducting electrodes for the memory cells which can be manufactured with microfabrication methods.

The object of the present invention is therefore to provide a method for the manufacturing of an electrode for use in organic semiconductor component and such that the electrode combines superior charge injection properties with a high conductivity. Furthermore it is an object of the invention to

provide a method which permits the manufacturing of an electrode of this kind with patterned line widths in the order of 1 μm. Finally it is also an object of the present invention to provide a method for manufacturing of electrodes which can be used in organic thin-film diodes, with high rectification ratio, or in electrode arrangements in organic thin-film transistors.

The above-mentioned objects and advantages are achieved by a method according to the invention which is characterized by depositing a first layer of a conducting or semiconducting material or combination of a conducting and a semiconducting material in the form of a patterned or non-patterned layer on an insulating substrate, such that at least a portion of the substrate is covered by the first layer, modifying the work function of the conducting and/or semiconducting material of the first layer by depositing a second layer of a conducting polymer with a work function higher than that of the material in the first layer such that the layer of the conducting polymer mainly covers the first layer or is conformal with the latter, whereby the combination of the first layer and the second layer constitutes the anode of the electrode arrangement and the work function of the anode becomes substantially equal to that of the conducting polymer, depositing a third layer of a semiconducting organic material on the top of the anode, and optionally and in case only a portion of the substrate is covered by the anode, also above at least some of the portion of the substrate not covered by the anode, and depositing a patterned or non-patterned fourth layer of a metal on the top of the third layer, whereby the fourth layer constitutes the cathode of the electrode arrangement.

It is according to the invention advantageous when the conducting material of the first layer is a metal and preferably the metal is selected among calcium, manganese, aluminium, nickel, copper or silver. It is also preferred that the semiconducting material of the first layer is selected among silicon, germanium or gallium arsenide.

In preferred embodiments of the method according to the invention the second layer can be deposited as a dispersion from a dispergent or as a dissolved material from solution or alternatively deposited in a melt-application process.

It is according to the method of the invention advantageous selecting the conducting polymer in the second layer on a doped conjugated polymer and then preferably selecting the conjugated polymer among poly(3,4-dioxyethylene thiophene) (PEDOT), a copolymer which includes the monomer, 3,4-dioxyethylene thiophene, substituted poly(thiophenes), substituted poly(pyrroles), substituted poly(anilines) or copolymers thereof., whereas the dopant for the conjugated polymer preferably is poly(4-styrene sulphonate) (PSS).

In a preferred embodiment of the method according to the invention the doped conjugated polymer as poly(3,4-ethylenedioxythiophene) (PEDOT) doped with poly(4-styrene sulphonate) (PSS).

It is according to the invention advantageous selecting the semiconducting organic material in the third layer among conjugated polymers, or crystalline, polycrystalline, microcrystalline and amorphous organic compounds, and in case the conjugated polymer is selected, it is preferred that this is selected among the conjugated polymer in the third layer among poly(2-methoxy, 5-(2'-ethylhexyloxi)-1,4-phenylene vinylene) (MEH-PPV) or poly(3-hexylthiophene) (P3HT).

Finally it is according to the invention advantageous selecting the metal of the fourth layer among metals which have a lower work function than that of the anode and then particularly selecting the metal of the fourth layer as the same as the metal selected for the first layer, but aluminium could in any case particularly be selected as the metal of the fourth layer.

The method according to the invention is used for manufacturing the electrode arrangement in an organic thin-film diode or for manufacturing electrode arrangements in a transistor structure, especially in an organic thin-film transistor a hybrid thin-film transistor.

The invention shall now be described in more detail with reference to the accompanying drawing as well as an appended example of polymer-based diodes with high rectification ratio manufactured according to the method described in the present invention.

Fig. 1a shows an example of the structure of a conducting polymer, viz. PEDOT-PSS.

fig. 1b an example of the structure of a conjugated polymer belonging to the class of polythiophenes, viz. P3HT,

fig. 1c an example of the structure of a conjugated polymer belonging to the class of polyphenylene vinylenes, viz. MEH-PPV,

fig. 2a a plan view of a first embodiment of a diode made according to the method of the present invention,

fig. 2b a plan view of another embodiment of a diode made according the method of the present invention,

fig. 2c a cross section through the diode in fig. 2b,

fig. 3a the current/voltage characteristics of a diode according to prior art manufactured according to two different processing protocols,

fig. 3b the current /voltage characteristics of a diode made by the method according to the present invention, and of a diode made according to prior art,

fig. 3c the current/voltage characteristics of a diode made by the method according to the present invention, and of a diode made according to prior art,

fig. 3d the current/voltage characteristics of a diode made by the method of the present invention. and of a diode made according to prior art,

fig. 3e the current/voltage characteristics of a diode made by the method according to the present invention, and of a diode made according to prior art,

fig. 3f the rectification ratio of a standard diode made by the method according to the present invention,

fig. 4 a semilog plot of the current voltage characteristics of a prior art diode and a diode according to the present invention, with insert showing the rectification ratio as a function of the voltage for the diode according to the present invention,

fig. 5 the forward current density of a 100 μm^2 diode according to the present invention scaled with the forward current density of the inventive diode in

fig. 4, with insert showing a semilog plot of the current/voltage characteristics of the 100 μm^2 diode, and

fig. 6 the forward current density of a 1 μm^2 diode according to the present invention scaled with the forward current density of the inventive diode in fig. 2, with insert showing a linear plot of the current/voltage characteristics of the 1 μm^2 diode.

The present invention can be used to realize electrode arrangements for organic semiconductor components in thin-film electronics. In the anode a conducting polymer is used in the form of a conjugated polymer to which has been added a suitable dopant. Fig. 1 shows a structure of such a conducting polymer where the conjugated polymer is poly(3,4-ethylenedioxythiophene) (PEDOT) doped with poly(4-styrenesulphonate) (PSS). This type of conducting polymer shall in the following be termed as PEDOT-PSS. Fig 1b shows the structure of a semiconducting conjugated polymer belonging to the class of polythiophenes, namely poly(3-hexylthiophene) (P3HT) and fig. 1c shows the structure of another semiconducting conjugated polymer, belonging to the class of polyphenylenevinylenes, namely poly(2-methoxy,5-(2'-ethylhexyloxy)-1,4-phenylenevinylene) (MEH-PPV). The use of these materials is well-known within organic semiconductor technology.

Fig. 2a shows a first embodiment of a diode in thin-film electronics made by the method according to the present invention. On a substrate 1 which is made by an electrically insulating material, e.g. glass or silicon where the surface is selectively oxidised to from silicon dioxide, there is patterned an electronic conductor with good conductivity, for example a metal in the form of thin stripes 2 which constitute a first layer 2 in the diode. The metal may be chosen among calcium, manganese, aluminium, nickel, copper or silver. Since the layer 2 constitutes a part of the anode in the diode, it might seem reasonable to select a metal with high work function value, for example Au or Pt as known in the prior art. However, these noble metals are more or less chemically inactive and at least as far as gold is concerned, also have a tendency to migrate into adjacent layers. Also gold should be avoided for reasons set out in the introduction. Therefore. according to the invention a metal with low work function shall be selected, for example copper, aluminium or silver which provide good adhesion to the overlying second

layer 3 which is made with a conducting polymer with high work function values. According to a preferred embodiment of the invention the second layer 3 employs a conducting polymer in the form of PEDOT doped with PSS. In fig. 2a this second layer 3 of PEDOT-PSS, is patterned conformally with the first layer 2, and the combination metal/PEDOT-PSS now constitutes the anode 2, 3 of the diode. Above the anode 2, 3 there is now provided a third layer 4 of a semiconducting polymer. According to a preferred embodiment of the invention the third layer is made of a semiconducting polymer, for instance preferably poly(2-methoxy,5-(2'-ethylhexyloxy)-1,4-phenylene vinylene) (MEH-PPV). Other semiconducting polymers may also be used, e.g. poly(3-hexylthiophene) (P3HT) may be relevant. Over the third layer 4 of semiconducting material the cathode 5 is now applied as a stripe electrode made from a metal with a suitably low work function value. This metal may e.g. be aluminium, but is not limited thereto and may in principle be made from other materials with comparable electronic properties, e.g. indium tin oxide (ITO). The diode in fig. 2a now appears as a sandwich structure with the anode made from several patterned stripe electrodes and shall be representative for embodiments where the active area, i.e. the semiconductor layer 4 typically is of the size in the order of 1 -100 μm^2.

Fig. 2b shows a diode structure where the metal layer in the anode 2, 3 is deposited unpatterned, e.g. on one half of the substrate 1. The conducting semiconductor 3 which again preferably may be PEDOT-PSS, is deposited mainly over the whole metal layer 2 and the anode 2, 3 is now realized and is well suited for use in high power diodes. Again, the active material 4 in the form of a semiconducting material is deposited over the anode 2, 3, with the cathode 5 on top, made from e.g. aluminium, deposited as two parallel wide stripes and forming the fourth layer in the diode structure. Fig. 2c shows a cross-section through the diode of fig. 2b cut along the line in the longitudinal direction through a cathode stripe 5. Typically the embodiment of the diode as shown in figs. 2b and 2c may represent a diode with an active area (i.e. the active semiconductor area 3) of the order of 6-10 mm^2.

In each case the embodiments of fig. 2 emerge as organic thin-film diodes in a sandwich construction.

Fig. 3a shows current/voltage characteristics of a prior art device in planar geometry made with PEDOT between copper electrodes, in that the curve with filled circles shows the characteristics of PEDOT spin-coated at 4000 rpm and the curve with open circles the characteristics of PEDOT spin-coated at 1000 rpm. The distance between the copper electrodes is approximately 1 mm and the characteristic is linear, which is typical of an ohmic resistance.

Fig. 3b shows the current/voltage characteristic expressed respectively through the forward current in the conducting direction and backward current in the blocking direction of a diode according to prior art (solid lines) and of a diode made according to the method of the present invention (lines with circles/dots). The known diode is made with P3HT as the semiconducting material, spin-coated at 600 rpm from a 5 mg/ml solution and arranged between a copper anode and an aluminium cathode, respectively. The current in the forward direction is shown by the upper solid line and the current in the backward direction by the lower solid line. The diode made by the method according to the present invention has an anode 2, 3 made from a double layer of copper and PEDOT-PSS as the conducting polymer, spin-coated at 3000 rpm. The active semiconducting material P3HT is spin-coated as 600 rpm from a 5 mg/ml solution, and the cathode is made from aluminium. In this case the characteristic has been determined through two measurement series, and as can be seen from fig. 2b the results are virtually identical. The respective measurement series are discerned through curves with open or closed circles, respectively. The two upper, almost coinciding curves exhibit the current in the forward direction, while the lower curves exhibit the current in the backward direction. The difference compared to the diode made by conventional means is obvious.

Correspondingly fig. 3c shows the current/voltage characteristics of a diode according to prior art and a diode made according to the present invention. The diode according to known art employs MEH-PPV spin-coated at 800 rpm from a 5 mg/ml solution as the semiconductor material, arranged in a sandwich between a copper anode and an aluminium cathode, respectively. Current/voltage characteristics are here represented by a curve with filled circles. The diode made according to the method of the present invention employs the same organic semiconductor material deposited under similar conditions, but again the anode is a double layer of copper with PEDOT-PSS

spin-coated at 4000 rpm, and the cathode is made from aluminium. The characteristics in this case are shown as a curve with open circles and the difference between the characteristics of the known component and the component made according to the method of the present invention are again obvious.

Fig. 3d shows in the same way as in fig. 3c the current/voltage characteristics of the same components, in that the conducting semiconductor and the active, organic semiconducting material are deposited under exactly the same conditions respectively, but in both cases the anode is now made with aluminium.

Fig. 3e shows the current/voltage characteristics of a diode according to prior art and a diode made by the method according to the invention. The known diode employs active material consisting of MEH-PPV spin-coated at 600 rpm from a 5 mg/ml solution and arranged in a sandwich between a nickel anode and an aluminium cathode. The characteristics are in this case shown by a curve with filled circles. The diode made by the method according to the present invention employs an anode made by a double layer of nickel and PEDOT-PSS spin-coated at 4000 rpm, while the active material is MEH-PPV spin-coated at 600 rpm from a 5 mg/ml solution, and the cathode is again aluminium. The characteristics are in this case shown by a curve with open circles.

Finally, fig. 3f shows the rectification ratio for a standard diode made by the method according to the present invention and with an anode in the form of a double layer of Cu/PEDOT-PSS, the active organic semiconductor in the form of MEH-PPV and with aluminium as the cathode. As can be seen, at voltages of 3 volt and above a rectification ratio as high as 10^6 - 10^7 is achieved.

According to the present invention anodes formed as double layers with metal, or alternatively a semiconductor or a semiconductor and a metal in combination, under a layer of a conducting polymer in the form of PEDOT-PSS shall improve the conductivity. The metal and the semiconductor in the anode may be Cu or Al which both possess a low work function, but in combination with PEDOT the anode appears with essentially the high work function of PEDOT. At the same time the combination of metal and PEDOT improves the conductivity of the anode. The PEDOT-PSS

layer modifies the injection properties of the anode metal which has a low work function value, providing a problem-free hole injection. If the anode were made from metal only, the current flow would be limited by the contact, but the use of PEDOT-PSS ensures that the current flow now shall be bulk-limited. Bu using a metal/PEDOT-PSS-anode it is, as shown in fig. 3f, possible to make diodes with a rectification ratio of up to seven orders of magnitude. A major advantage which is achieved by employing an anode of metal and a conducting polymer, is the possibility of being able to pattern the anode. The use of metal under PEDOT yields higher conductivity along the electrodes compared to the conducting polymer itself. Even with patterned electrodes with line widths of the order of 1 μm, high current density can be achieved in combination with superior charge injection properties. This can be used to realize memory cells in polymer memories with high data storage density and it becomes possible to achieve high read-out speeds because of the highly conducting electrodes. At the same time the memory cells may be realized with line widths in the order of 1 μm by suitable patterning of the metal/polymer layer. In this connection it should be remarked that the contact between any metal in the anode and a highly doped conducting polymer shall be ohmic.

Below follows examples of diodes made by the method according to the present invention and the associated current/voltage characteristics that have been achieved, and associated figures.

Example

A large effort has been undertaken towards fabrication of electronic devices using polymers. Most of these are directed towards field effect transistors and diodes, in imitation of silicon electronics. Among the diodes, both light emitting diodes and light detecting diodes constitute the major fraction of the studies; in both of these a transparent electrode is suitable. However, a high rectification organic diode is quite important for a broad spectrum of electronic applications. In order to fabricate diodes based on semiconducting polymers with high rectification, one needs materials that allow efficient charge injection trough the polymer under forward bias, and much less so under reverse bias. Normally this is achieved using materials that match in energy position, or make low potential barriers, to the HOMO (Highest Occupied Molecular Orbital) and LUMO (Lowest Unoccupied Molecular Orbital) levels of the polymer. In the reverse bias both barriers for electrons

and holes must be high enough to keep the current low, having thus as a result a high rectification ratio. But it is not just the energy levels that matter. The interface properties and the quality of the polymer film formed onto a given metal can define the diode properties; often polymer film spin-coated onto inert materials such as gold presents pin holes that is not acceptable, if one needs to evaporate an upper electrode on top of the polymer film, in a sandwich geometry. The conducting/semiconducting polymer interface tends to have good adhesion. The oxidized conducting polymer poly(3,4-ethylenedioxythiophene) doped with poly(4-styrenesulphonate) (PEDOT-PSS) was found to have the high work function value 5,2 eV which allows efficient hole injection in LEDs or collectors in photodiodes. However, the higher resistance of PEDOT-PSS compared with ordinary metals may compromise the diode performance in thin patterned lines, due to voltage drop under high currents. To handle this problem, a metal layer under the polymer is used. Any metal can be used as the underlying layer as it is not necessary to mach the work function of the metal (ϕ_m) with the work function of PEDOT (ϕ_{PEDOT}). Diodes made with several metals (Al (4,2 eV), Ag (4,3 eV), Cu (4,5 eV)) were tested. In all cases the current flow of holes which was contact-limited, changed to bulk-limited when a PEDOT-PSS layer was used between the anode metal and the semiconducting polymer MEH-PPV (poly(2-methoxy, 5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene)). In order to study the electrical properties of diodes with different active areas copper was chosen as the underlying layer, particularly due to its good stability and etching properties. The Cu/PEDOT-PSS interface was demonstrated to be ohmic with a contact resistance $r_c \approx 7\ \Omega/\square$. The ohmic behaviour of Cu/PEDOT-PSS interface is an important asset for its use as an electrode in diodes. The contact resistance of Cu/PEDOT-PSS interface was measured using planar geometry to provide a copper surface similar to that used for the diodes.

The diodes were constructed in sandwich geometry using Cu/PEDOT-PSS as the anode and Al as the cathode ($\phi = 4.2$ eV). They were mounted onto a glass or Si with 2 μm thick oxide substrate, as shown in figs. 2a-c. Figure 2b shows the geometry for the ordinary diodes, usually with 6-10 mm^2 active area. For these diodes the copper layer was deposited by evaporation to a preferred thickness of 200 nm onto one half of the substrate. The PEDOT-PSS (Bayer AG, Germany) layer with a thickness of 80 nm, was

deposited by spin-coating from a solution of water with 30% isopropanol, and filtered a using 1 μm pore glass filter. The PEDOT-PSS was patterned conformally onto the copper and then annealed for 5 min. in 120° C. It was noticed that the PEDOT-PSS solution reacts with copper oxide, etching the surface of the Cu film, which eases the formation of the contact. The semiconducting polymer layer was deposited by spin-coating using a MEH-PPV polymer dissolved into chloroform at the concentration of 5mg/ml, to a thickness of 190 nm. The second electrode Al was vacuum evaporated through a shadow mask defining the active area. For the diodes with 1 μm^2 and 10 μm^2 of active area the construction followed the patterning steps common in the Si technology. The processing includes patterning of Cu layer (200 nm thick) with PEDOT-PSS (80 nm thick) on top in 500 μm long stripes with width of 1 μm and 10μm, followed by the annealing treatment. This patterned substrate was covered with MEH-PPV by spin-coating and Al was sputtered on top and patterned in stripes similar to Cu in order to make intersections of 1 μm^2 and 100 μm^2. The geometry of a diode of this kind is presented in fig. 1b.

The I-V characteristics of two similar diodes made using MEH-PPV polymer is presented in fig. 4, which shows a semilog plot of the current voltage characteristics of a MEH-PPV-based diode using a copper anode (open circles) and a similar MEH-PPV-based diode using a Cu/PEDOT-PSS anode (solid circles). The insert graph here shows a semilog plot of the rectification ratio versus the voltage for the diode with the Cu/PEDOT-PSS anode. The measurements were performed using a Hewlett Packard 4156A precision semiconductor parameter analyser in dark environment. It is possible to notice the difference in the shape of the current-voltage dependence regarding the inclusion of the PEDOT-PSS layer. Due to higher value of the work function of PEDOT-PSS (5.2 eV) compared to Cu (4.5 eV), the energy barrier for hole injection from PEDOT-PSS to the MEH-PPV is $\varphi \cong 0.1$ eV. This is much smaller than that from Cu to MEH-PPV which is $\varphi \cong 0.8$ eV, [1] as the current limitation in this two situations are different. Copper presents a contact-limited current regime; in this low injection regime the current densities are small and space charge effects can be neglected. With the inclusion of a thin layer of PEDOT-PSS it will be possible to make a transition to a bulk-limited current regime where the forward current is mostly due to the positive carriers coming from the Cu/PEDOT-PSS

electrode. The Cu/PEDOT-PSS/MEH-PPV/Al diodes presented a J(V) function with three limiting regions, J being the current density. From 0 to 1 volt the current is at the noise level of the equipment: little charge flow occurs. This condition is due to the difference in the work function values of the electrodes PEDOT-PSS and Al ≅ 1eV) which creates an inherent potential in the polymer layer that opposes hole injection. One first has to apply this voltage in order to inject charge. Between 1 and 2 volts the current has an exponential behaviour, and increases by five orders of magnitude. This dramatic increase is a property of the interface PEDOT-PSS/MEH-PPV with its low energy barrier. Beyond 2 volts the current becomes dependent on the transport properties of the MEH-PPV layer. The insert graph in fig. 4 shows the rectification ratio value of this diode as a function of voltage, the rectification ratio being taken by dividing the forward by the reverse current. At 3 volts it already shows a rectification ratio of six orders of magnitude, increasing to seven between 4 and 8 volts. Beyond 8 volts the injection of holes from Al to MEH-PPV increases the reverse current decreasing the rectification ratio value.

Fig. 5 shows the forward current density of a 100 μm^2 diode according to the invention and with Cu/PEDOT-PSS/MEH-PPV/Al structure (solid triangles) scaled with the forward current density (solid circles) of the diode according to the invention as shown in fig. 4, while the insert graph shows a semilog plot of the current voltage characteristics of the 100 μm^2 diode.

The Cu/PEDOT-PSS/MEH-PPV/Al diodes with 100 μm^2 of active area presented similar shape of the forward current-voltage characteristics, as can be seen in the insert graph in fig 5. In order to compare the I-V characteristics of both diodes, the current density are plotted in fig. 5 both for the diode in fig. 4 (8 mm^2) and for the diode with 100 μm^2. The shift in the absolute value of the current can be understood due to the thickness difference between the diodes. The scaling is quite consistent.

Fig. 6 shows the forward current density of a 1 μm^2 diode according to the present invention and with a Cu/PEDOT-PSS/MEH-PPV/Al structure (open squares) scaled with a forward current density of the diode (solid circles) according to the invention in fig. 4, while the insert graph shows a linear plot of the current voltage characteristics of the 1 μm^2 diode.

However, for a diode of this size the current level is quite low, around the noise level as can be seen in the insert graph in fig. 5. The I-V characteristics for the current density of both the diode with 1 μm^2 active area and the one of 8 mm^2 active area are plotted. The function J(V) for the smaller diode is plotted up to twenty volts. It will be seen that its behaviour and shape do not scale very well with the larger diode. In these small diodes, the area extension is only ten times the thickness of the layers, and fringe fields are expected to start becoming important; even more important may be the existing irregularities causing any geometrical estimates to err.

The electrical transport properties of conjugated polymers and polymer/metals junctions has been studied for quite some time. The first attempt in modelling the PPV^- based diodes were based on the Fowler-Nordheim model describing the tunnelling process in the diode. It was possible to obtain the approximate values for barrier heights and for the polymer energy levels. A number of models has since then been presented taking in account more parameters for detailing the interface properties. It is proposed that when the current is contact-limited it can be determined by the image force, the effect of Coulomb trapping of carriers at the interface. This trapping results in an increase of the energy barrier height, decreasing the injection flow. It was concluded that the presence of an insulating material free of traps could increase the charge injection. In the case of PEDOT-PSS it was shown that during the deposition of this material by spin-coating a segregation of PEDOT and PSS takes place. PSS is an insulating material and it was found to form a thin layer all over the PEDOT surface film. This thin layer cannot trap charges from the electrode which may account for the improvement in the carrier injection from PEDOT. The bulk-limited current of MEH-PPV has been studied and reported by several research groups. It was found that at high fields MEH-PPV presents a spatial charge limitation of the current, and also that mobility is dependent on the applied electric field. In the present case the behaviour is similar, as the current does not depend on V^2 precisely because of the field-dependent mobility. This was proposed in a recent study by Malliaras & al., PRB, Vol 58, R13411 (1998). The use of a model developed by P. N Murgatroyd (J.Phys. D. Vol. 3, 151 (1970)) combines spatial charge limitation dependence with the non-constant mobility in the same equation. From these models one can evaluate the data obtained herein by plotting the high field current in the function format JL^3 versus (VL), where J is the current density, L the polymer thickness and V the

applied voltage minus the built-in voltage of the diodes. For the present invention this enabled a data fit and gave similar values for the polymer parameters μ_0 and E_0, i.e. the zero field mobility and the characteristic field respectively.

In summary, the present invention provides a high rectification ratio polymer diode using two low work function metals, where the anode was modified by the introduction of a conducting polymer layer, PEDOT doped with PSS. With this surface modification it was possible to progress from a low injection contact-limited current to a high injection bulk-limited current. The PEDOT/PSS segregation might add to the charge injection by avoiding Coulomb trapping at the interface due to the force image effects. The possibility of making these diodes patterned on micrometer scale has been shown. This offers the prospect of fabricating such diodes for microelectronics with active devices such as switching diodes and switching transistors, but also in electrically addressable high-density thin-film memories in e.g. a passive matrix.

PATENT CLAIMS

1. A method in the fabrication of an organic thin-film semiconducting device, wherein the semiconducting device comprises an electrode arrangement with electrodes contacting a semiconducting organic material, and wherein the method is characterized by
depositing a first layer of a conducting or semiconducting material or combination of a conducting and a semiconducting material in the form of a patterned or non-patterned layer on an insulating substrate, such that at least a portion of the substrate is covered by the first layer
modifying the work function of the conducting and/or semiconducting material of the first layer by depositing a second layer of a conducting polymer with a work function higher than that of the material in the first layer such that the layer of the conducting polymer mainly covers the first layer or is conformal with the latter, whereby the combination of the first layer and the second layer constitutes the anode of the electrode arrangement and the work function of the anode becomes substantially equal to that of the conducting polymer,
depositing a third layer of a semiconducting organic material on the top of the anode, and optionally and in case only a portion of the substrate is covered by the anode, also above at least some of the portion of the substrate not covered by the anode, and
depositing a patterned or non-patterned fourth layer of a metal on the top of the third layer, whereby the fourth layer constitutes the cathode of the electrode arrangement.

2. A method according to claim 1,
characterized by the conducting material of the first layer being a metal.

3. A method according to claim 2,
characterized by selecting the metal among calcium, manganese, aluminium, nickel, copper or silver.

4. A method according to claim 1,
characterized by selecting the semiconducting material of the first layer among silicon, germanium or gallium arsenide.

5. A method according to claim 1,
characterized by depositing the second layer as a dispersion from a dispergent or as a dissolved material from a solution.

6. A method according to claim 1,
characterized by depositing the second layer in a melt application process.

7. A method according to claim 1,
characterized by selecting the conducting polymer in the second layer on a doped conjugated polymer.

8. A method according to claim 7,
characterized by selecting the conjugated polymer among poly(3,4-dioxyethylene thiophene) (PEDOT), a copolymer which includes the monomer, 3,4-dioxyethylene thiophene, substituted poly(thiophenes), substituted poly(pyrroles), substituted poly(anilines) or copolymers thereof.

9. A method according to claim 7,
characterized by selecting the dopant for the conjugated polymer as poly(4-styrene sulphonate) (PSS).

10. A method according to claims 7 and 8,
characterized by selecting as the doped conjugated polymer as poly(3,4-ethylenedioxythiophene) (PEDOT) doped with poly(4-styrene sulphonate) (PSS).

11. A method according to claim 1,
characterized by selecting the semiconducting organic material in the third layer among conjugated polymers, or crystalline, polycrystalline, microcrystalline and amorphous organic compounds.

12. A method according to claim 11,
characterized by selecting the conjugated polymer in the third layer among poly(2-methoxy, 5-(2'-ethylhexyloxi)-1,4-phenylene vinylene) (MEH-PPV) or poly(3-hexylthiophene) (P3HT).

13. A method according to claim 1,
characterized by selecting the metal of the fourth layer among metals which have a lower work function than that of the anode.

14. A method according to claim 13, characterized by selecting the metal of the fourth layer as the same as the metal selected for the first layer.

15. A method according to claim 14, characterized by selecting aluminium as the metal of the fourth layer.

16. Use of the method according to any of the claims 1-15 for manufacturing the electrode arrangement in an organic thin-film diode.

17. Use of the method according to any of the claims 1-15 for manufacturing the electrode arrangement in a transistor structure, especially in an organic thin-film transistor or a hybrid thin-film transistor.

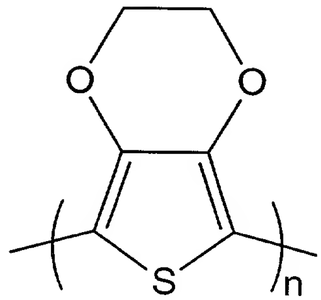


Fig. 1a

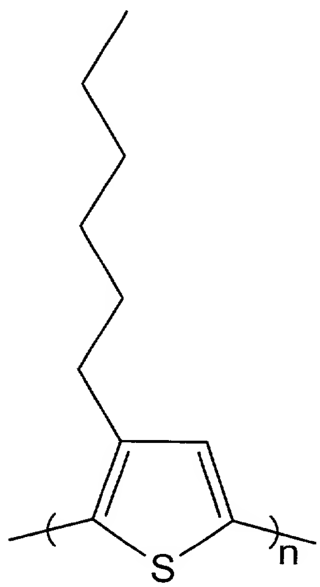


Fig. 1b

$R_1 = CH_2CH(C_2H_5)C_4H_9$
$R_2 = CH_3$

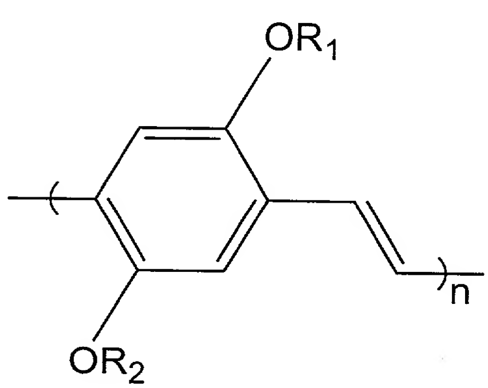


Fig. 1c

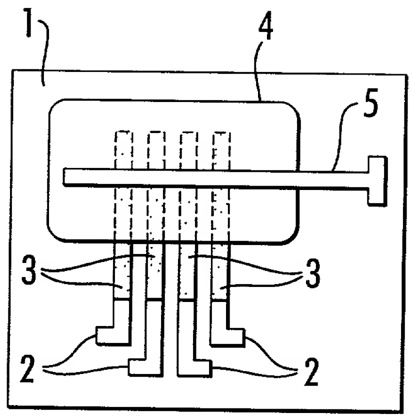


Fig.2a

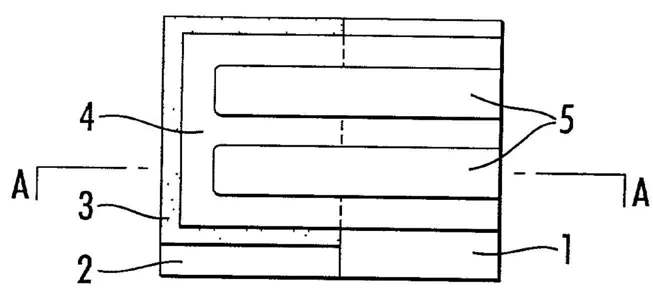


Fig.2b

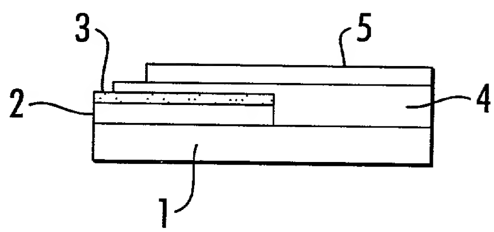


Fig.2c

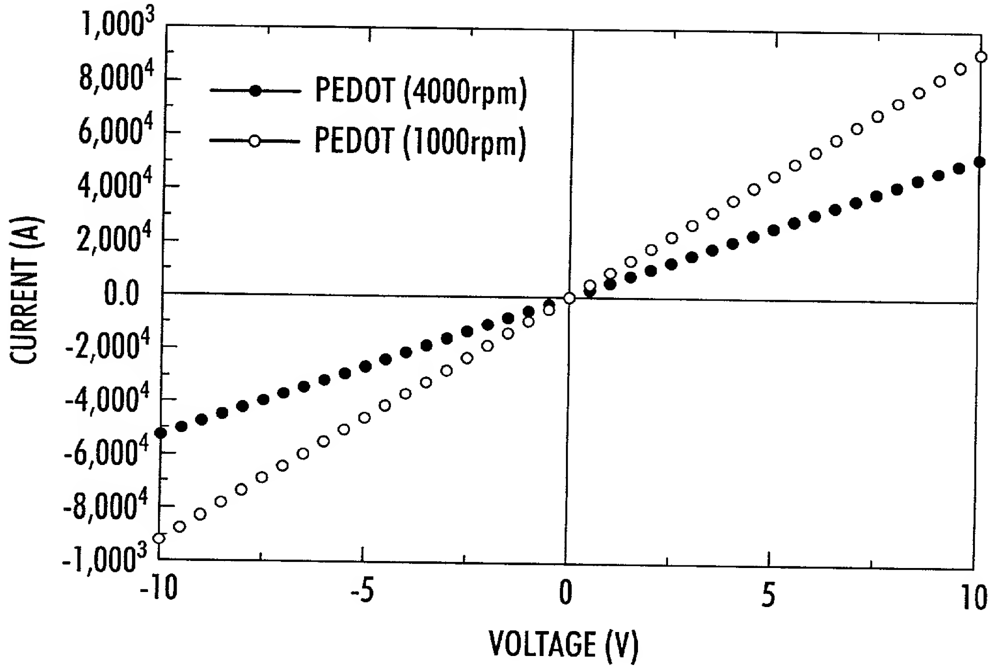

1,000³
8,000⁴
6,000⁴
4,000⁴
2,000⁴
0.0
-2,000⁴
-4,000⁴
-6,000⁴
-8,000⁴
-1,000³
CURRENT (A)
PEDOT (4000rpm)
PEDOT (1000rpm)
-10
-5
0
5
10
VOLTAGE (V)

Fig.3a

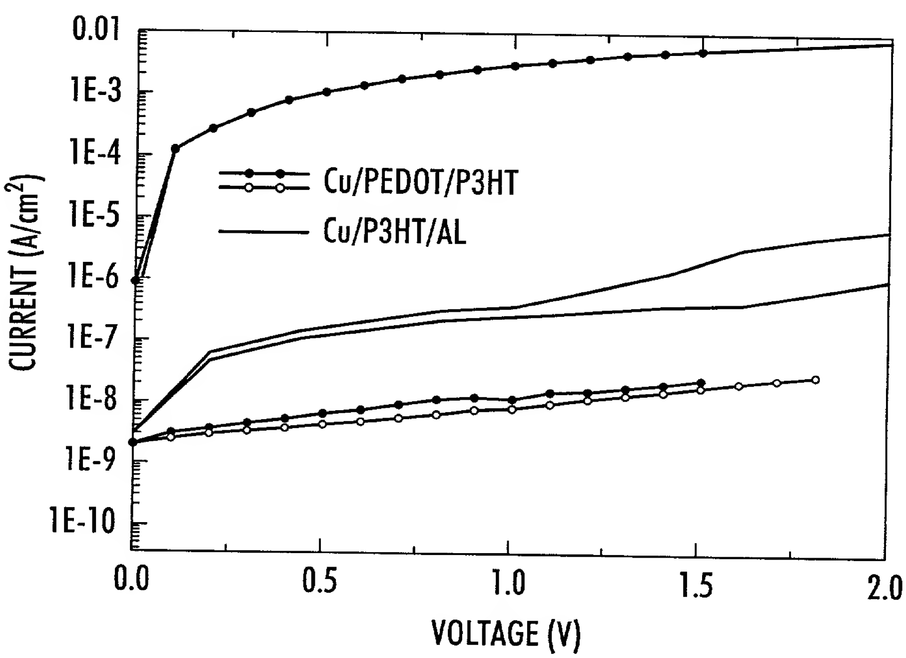
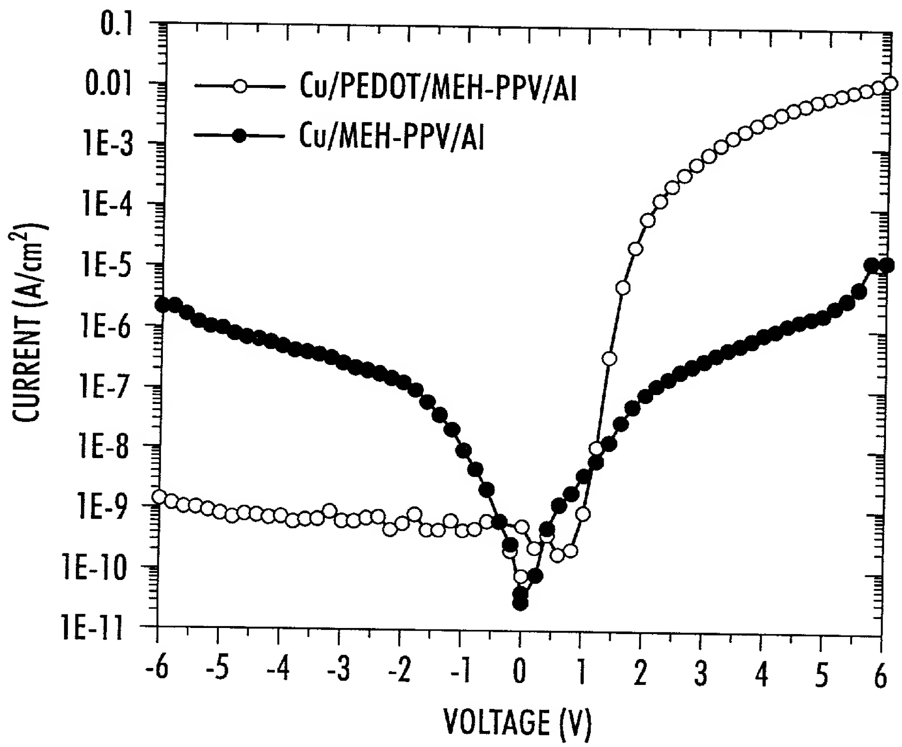
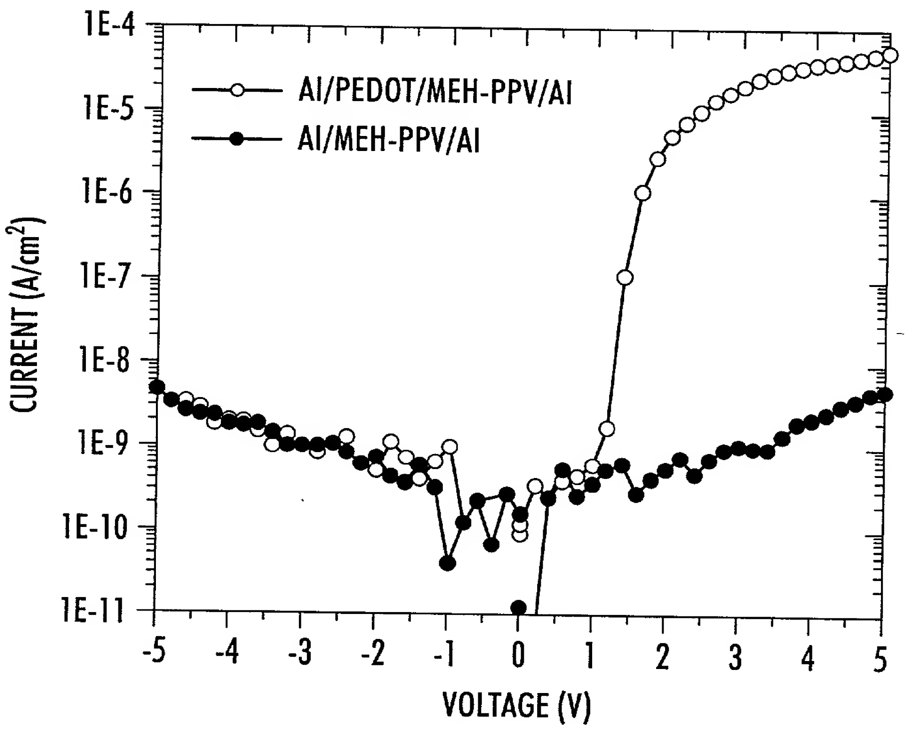

0.01
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
CURRENT (A/cm²)
Cu/PEDOT/P3HT
Cu/P3HT/AL
0.0
0.5
1.0
1.5
2.0
VOLTAGE (V)

Fig.3b



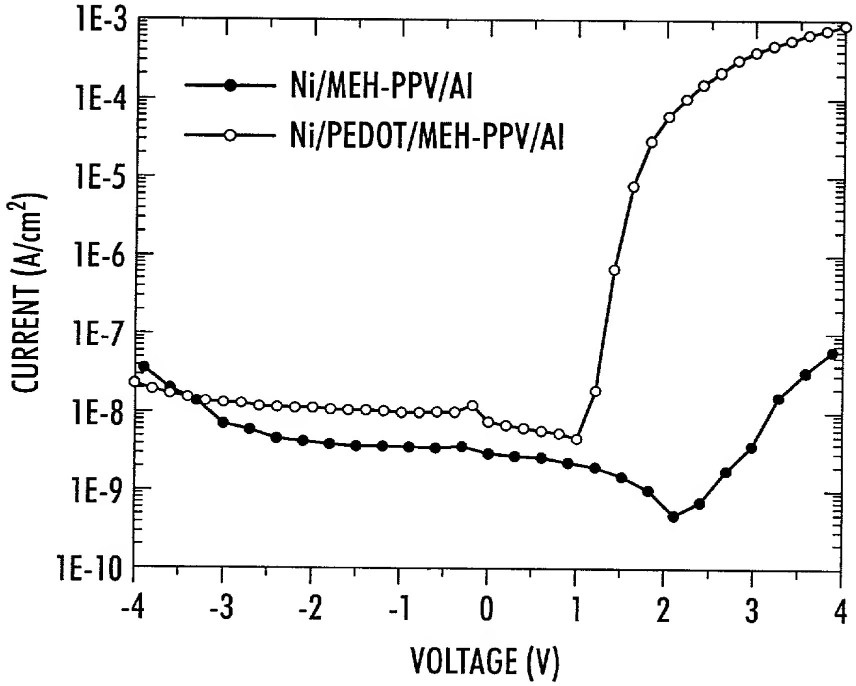
0.1
0.01
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
Cu/PEDOT/MEH-PPV/Al
Cu/MEH-PPV/Al
CURRENT (A/cm^2)
-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
VOLTAGE (V)

Fig.3c



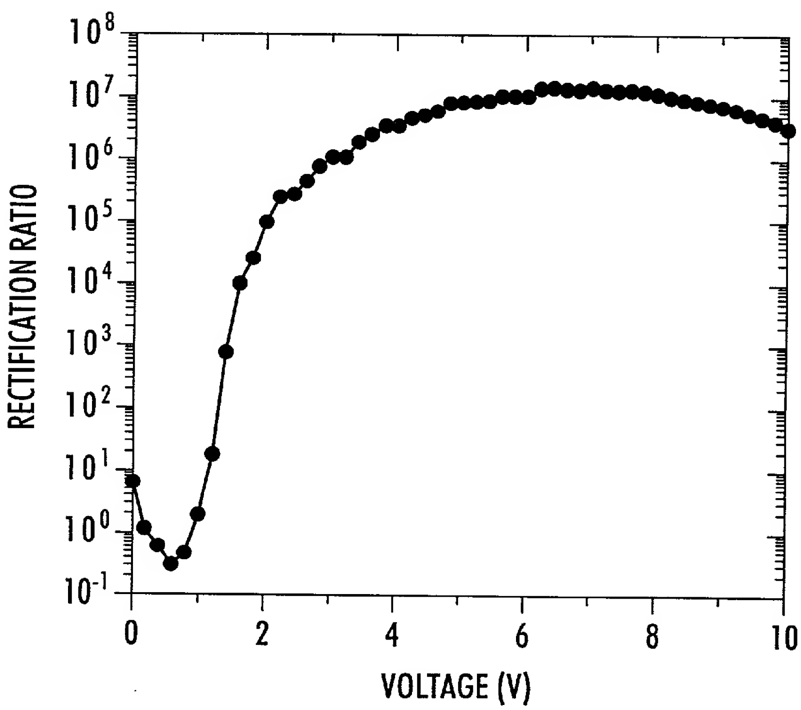
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
Al/PEDOT/MEH-PPV/Al
Al/MEH-PPV/Al
CURRENT (A/cm^2)
-5 -4 -3 -2 -1 0 1 2 3 4 5
VOLTAGE (V)

Fig.3d



1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
CURRENT (A/cm^2)
Ni/MEH-PPV/Al
Ni/PEDOT/MEH-PPV/Al
-4
-3
-2
-1
0
1
2
3
4
VOLTAGE (V)

Fig.3e



10^8
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0
10^{-1}
RECTIFICATION RATIO
0
2
4
6
8
10
VOLTAGE (V)

Fig.3f

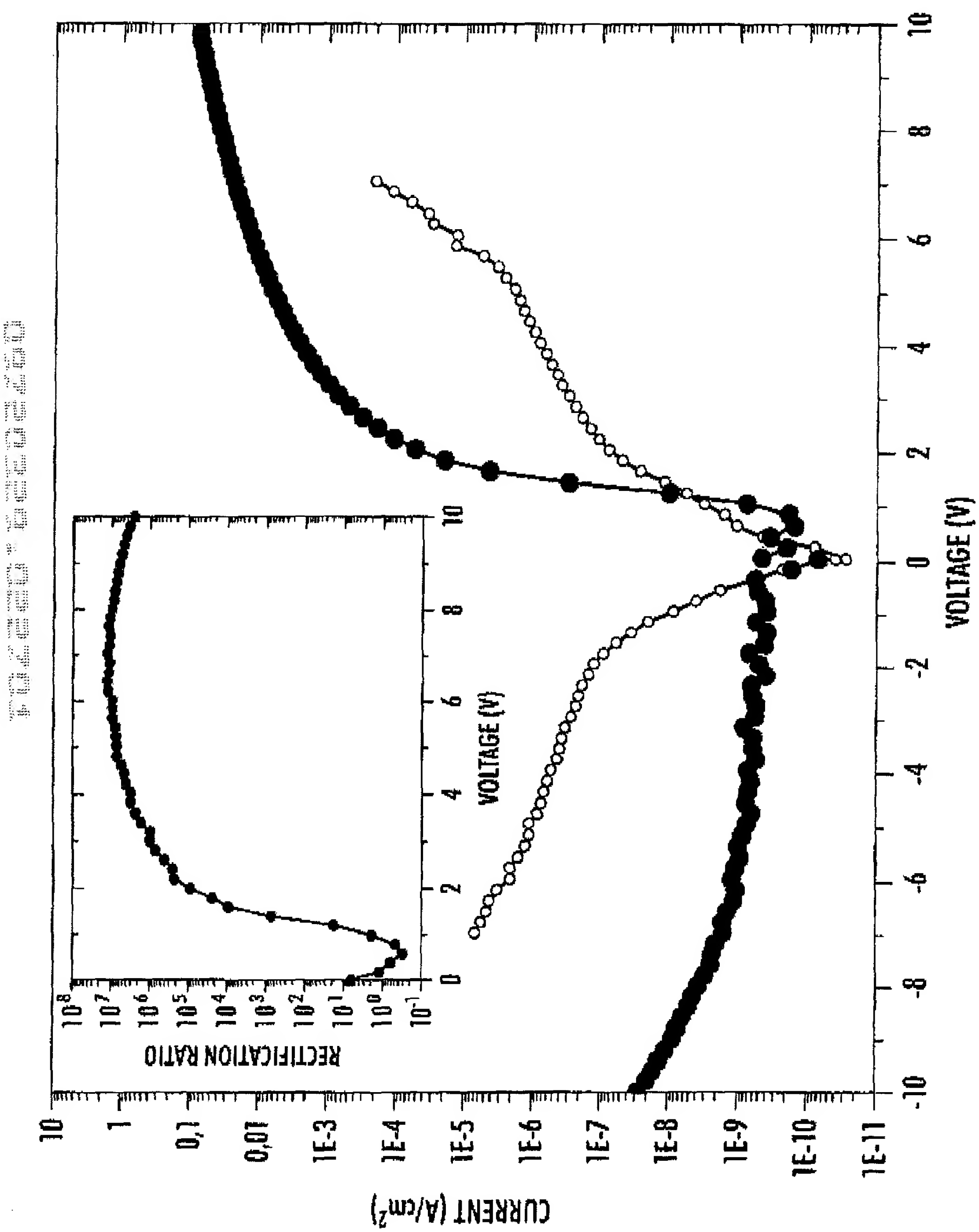
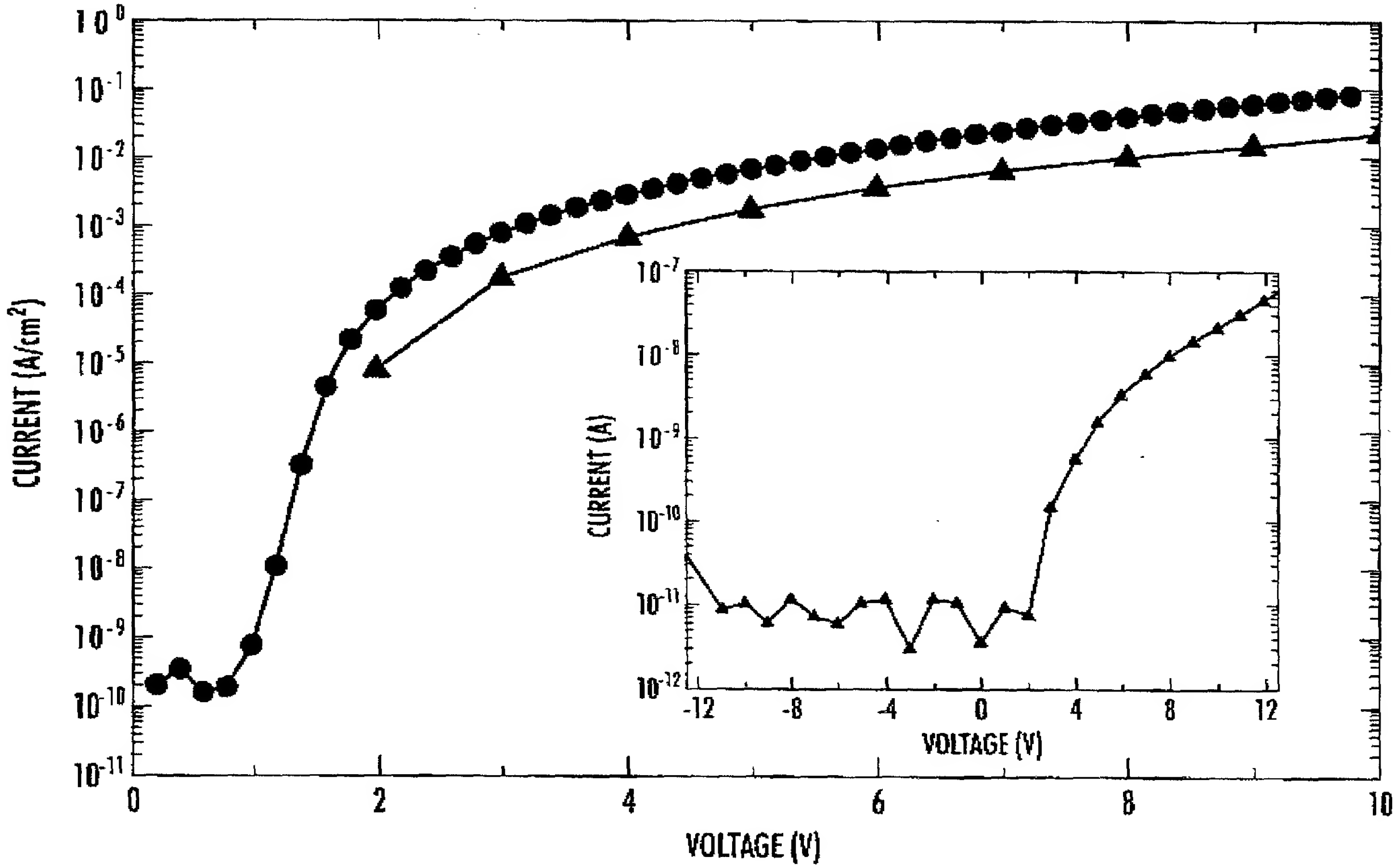

CURRENT (A/cm^2)
10
1
0,1
0,01
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
VOLTAGE (V)
-10
-8
-6
-4
-2
0
2
4
6
8
10
RECTIFICATION RATIO
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10^{1}
10^{0}
10^{-1}
VOLTAGE (V)
0
2
4
6
8
10

Fig.4



CURRENT (A/cm²)
10⁰
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
10⁻⁸
10⁻⁹
10⁻¹⁰
10⁻¹¹
0
2
4
6
8
10
VOLTAGE (V)
CURRENT (A)
10⁻⁷
10⁻⁸
10⁻⁹
10⁻¹⁰
10⁻¹¹
10⁻¹²
-12
-8
-4
0
4
8
12
VOLTAGE (V)

Fig.5

09/720329

8/8

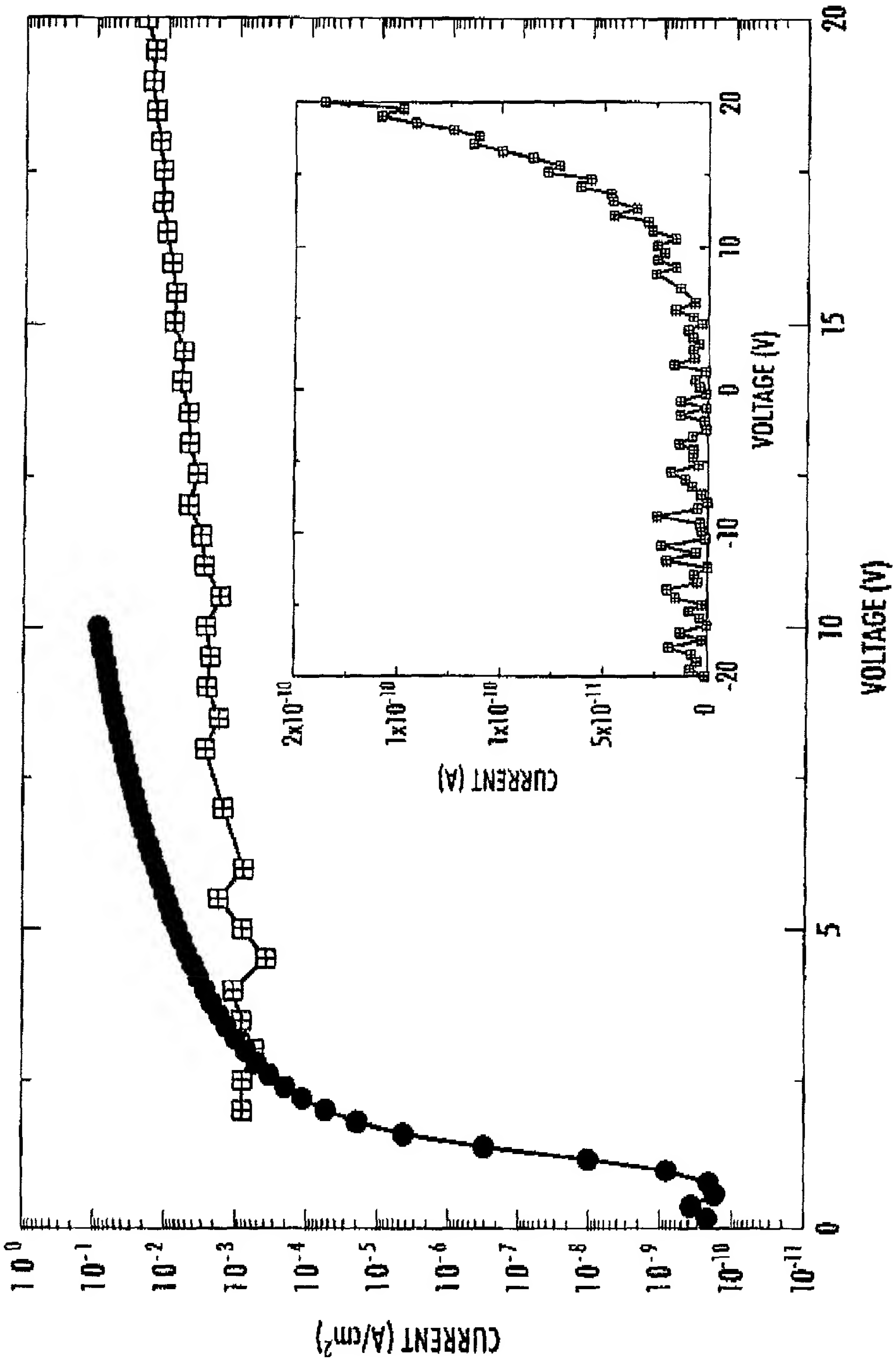


Fig.6

Attorney Docket No. 3672-0110P

BIRCH, STEWART, KOLASCH & BIRCH, LLP
P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

COPY

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: A METHOD IN THE FABRICATION OF ORGANIC THIN-FILM SEMICONDUCTING DEVICES

Fill in Appropriate Information - For Use Without Specification Attached:

the specification of which is attached hereto. If not attached hereto,
the specification was filed on ________ as
United States Application Number ________;
and amended on ________ (if applicable) and/or
the specification was filed on April 14, 2000 as PCT
International Application Number PCT/NO00/00127; and was
amended under PCT Article 19 on ________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)

Prior Foreign Application(s) — Priority Claimed

(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
19991916	Norway	April 22, 1999	☒	☐
			☐	☐
			☐	☐
			☐	☐

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below.

Insert Provisional Application(s): (if any)

(Application Number) (Filing Date)

(Application Number) (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Insert Requested Information: (if appropriate)

Country	Application Number	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S. Application(s): (if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Raymond C. Stewart	(Reg. No. 21,066)	Terrell C. Birch	(Reg. No. 19,382)
Joseph A. Kolasch	(Reg. No. 22,463)	James M. Slattery	(Reg. No. 28,380)
Bernard L. Sweeney	(Reg. No. 24,448)	Michael K. Mutter	(Reg. No. 29,680)
Charles Gorenstein	(Reg. No. 29,271)	Gerald M. Murphy, Jr.	(Reg. No. 28,977)
Leonard R. Svensson	(Reg. No. 30,330)	Terry L. Clark	(Reg. No. 32,644)
Andrew D. Meikle	(Reg. No. 32,868)	Marc S. Weiner	(Reg. No. 32,181)
Joe McKinney Muncy	(Reg. No. 32,334)	Donald J. Daley	(Reg. No. 34,313)
John W. Bailey	(Reg. No. 32,881)	John A. Castellano	(Reg. No. 35,094)
Gary D. Yacura	(Reg. No. 35,416)		

17

Send Correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP or **Customer No. 2292**
P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING: ↓

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor: Insert Name of Inventor Insert Date This Document is Signed → Insert Residence Insert Citizenship → Insert Post Office Address → 1W

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Lucimara Stolz ROMAN		2001/01/17
Residence (City, State & Country)	CITIZENSHIP	
Linköping, Sweden SEX	BRAZILIAN	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Mårdtorpsgatan 29, S-584 32 LINKÖPING SWEDEN		

Full Name of Second Inventor, if any: see above 2W

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Olle INGANÄS		2000/12/08
Residence (City, State & Country)	CITIZENSHIP	
Linköping Sweden SEX	SWEDISH	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Wernersgatan 13, S-582 35 LINKÖPING SWEDEN		

Full Name of Third Inventor, if any: see above 3W

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Olle HAGEL		2001/01/02
Residence (City, State & Country)	CITIZENSHIP	
Linköping Sweden SEX	SWEDISH	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Lektorsgatan 3, S-582 35 LINKÖPING SWEDEN		

Full Name of Fourth Inventor, if any: see above 4W

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Johan CARLSSON		2000/12/11
Residence (City, State & Country)	CITIZENSHIP	
Linköping Sweden SEX	SWEDISH	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Ekholmsvägen 219, S-589 29 Linköping Sweden		

Full Name of Fifth Inventor, if any: see above 5W

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Göran GUSTAFSSON		2000/12/11
Residence (City, State & Country)	CITIZENSHIP	
Linköping Sweden SEX	SWEDISH	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Trumslagaregatan 33, S-582 16 Linköping Sweden		

Attorney Docket No.

Full Name of Sixth Inventor, if any: see above

6W

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE		DATE*
Magnus BERGGREN			2000/12/28
Residence (City, State & Country)		CITIZENSHIP	
Vreta Kloster, Sweden SE		SWEDISH	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
Bergsbadsvägen 14, S-590 77 Vreta Kloster, Sweden			

Page 3 of 3
(Rev. 01/05/2000)

*DATE OF SIGNATURE